

ABSTRACT OF THE DISCLOSURE

A write-bank selecting unit selects different memory banks in response to $N+1$ consecutive write requests, respectively. In each memory cycle, a data writing unit inputs N or less write commands to a data access unit. On the other hand, a primary read-bank selecting unit selects readable memory banks in each memory cycle. A secondary read-bank selecting unit selects memory banks corresponding to read requests for which data blocks could not be read out in the preceding memory cycle. A data reading unit generates read commands for those read banks and inputs the generated read commands to a data access unit. With this configuration, a packet buffer capable of satisfying both of short processing cycles and high memory use efficiency can be provided by using memory devices at a relatively low price.